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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/820,435	BELLANTONI ET AL.
	Examiner	Art Unit	
	Jonathan R. Plante	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 April 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>17 December 2004</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   The instant application having Application Number: 10/820,435 has a total of 26

claims pending in the application; there are 2 independent claims and 24 dependent

claims, all of which are ready for examination by the examiner.

Oath/Declaration

2.   The applicant's oath/declaration has been reviewed by the examiner and is found

to conform to the requirements prescribed in **37 C.F.R. 1.63.**

Drawings

3.   The drawings are objected to because:

a.   Please insert "**178**" into FIG. 1B for reference to "**OBJECT API**" as

referenced in (Paragraph 0027, Line 21).

b.   FIG. 1C includes the following reference character "112" that is not

referenced in the description.

c.   Please replace "**SOFTWARE OBJECTS**" (FIG. 2) with "HARDWARE

OBJECTS" to be in agreement with specifications "Broadly, a plurality of

hardware objects 202_1, 202_2 are initially provided" (Paragraph 0029, Line 8), and

"hardware objects (e.g. the objects 202_1, 202_2 as shown)" (Paragraph 0031, Line

5).

d.   Please change "**UPDATE**" (FIG. 2, 210) to "UPDATE OBJECT" to match

(FIG. 1B, 210).

e.   Please resolve indexing of 210 "**UPDATE OBJECT**" (FIG. 1B) between

drawing and specification. Specification reads "**an update command 210**"

(Paragraph 0029, Line 12), "**an update command 210**" (Paragraph 0032, Line

2), "**the update command 210**" (Paragraph 0033, Line 1), "**the update**

command 210" (Paragraph 0032, Line 3).

f.   Please move index "**220**" (FIG. 2) to be in proximity of "**SOURCE**

VARIABLE" (FIG. 2) for clarification.

g.   Please move index "**242**" (FIG. 2) to be in proximity of "**DESTINATION**

VARIABLE" (FIG. 2).

h.   Please replace "**CPU OBJECT**" (FIG. 3A, 304) with "HARDWARE

OBJECT" to be in agreement with specification "for a hardware object 304"

(Paragraph 0035, Line 6), "hardware objects 304" (Paragraph 0037, Line 2), and

"the hardware objects 304" (Paragraph 0037, Line 6).

i.   Please replace "**CPU OBJECT**" (FIG. 3B, 304) with "HARDWARE

OBJECT" to be in agreement with specification "the hardware objects 304"

(Paragraph 0038, Line 2)

j.   Please insert "**342**" in FIG. 3B for reference to "**INTERCONNECTION**

OBJECT" as referenced in (Paragraph 00387, Line 20).

k.   FIG. 4 includes the following reference characters/numbers "1, 2, and 3"

that are not referenced/defined in the specification. Please define "1, 2, and 3".

l.   FIG. 4 Please replace "**HW OBJECT**" with "HARDWARE OBJECT".

m.   FIG. 4. Please replace "**SW OBJECT**" with "SOFTWARE OBJECT".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4.   The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Suggested new title is "System-Level Object-Oriented Hardware Simulation of Devices Having Asynchronous Timing" to reflect the applicants focus on object-oriented programming to represent the hierarchal hardware in the simulation. (Applicant is reminded that application titles can consist of 500 or fewer characters)

5.   The disclosure is objected to because of the following informalities:

a.   Please insert "object-oriented hierarchal hardware simulation" into the

abstract to accurately reflect the scope the application.

b.   Please insert "synchronous" and asynchronous" into the abstract to

accurately reflect the scope to the application.

c.   Please replace "**times, e.g., in response to an appropriate transition.**"

(Paragraph 0008, Line 9) with "times (e.g., in response to an appropriate

transition)."

d.   Please replace "**into API-accessible,**" (Paragraph 0015, Line 7) with "into

application programming interface (API) accessible,".

e.   Please replace "**FIFO buffer**" (Paragraph 0015, Line 9) with "First In First

Out (FIFO) buffer".

f.   Please replace "**i.e., written expressly for interaction with the system**

environment." (Paragraph 0018, Line 7) with "(i.e., written expressly for

interaction with the system environment)."

g.   Please replace "**the objects**" (Paragraph 0018, Line 40) with "the

hardware objects".

h.   Please replace "**the objects**" (Paragraph 0018, Line 42) with "the

hardware objects".

i.   Please replace "**method 100,**" (Paragraph 0019, Line 7) with "method

FIG. 1A, 100".

j.   Please replace "**the object**" (Paragraph 0023, Line 1) with "the hardware object".

k.   Please replace "**Once the object**" (Paragraph 0020, Line 12) with "Once the hardware object".

l.   Please replace "**initialized, the object**" (Paragraph 0020, Line 12) with "initialized, the hardware object".

m.   Please replace "**used, i.e., a system-level model interacts through a wrapper with a hardware object.**" (Paragraph 0026, Line 2) with "used (i.e., a system-level model interacts through a wrapper with a hardware object)."

n.   Please replace "**the object**" (Paragraph 0026, Line 23) with "the hardware object".

o.   Please replace "**parallelism, e.g., avoiding "race conditions."**" (Paragraph 0032, Line 13) with "parallelism (e.g., avoiding "race conditions")."

p.   Please replace "**steps, e.g., storing the data and then flowing it upon receipt of an update command,**" (Paragraph 0032, Line 36) with "steps (e.g., storing the data and then flowing it upon receipt of an update command)"

q.   Please replace "**POSIX**" (Paragraph 0032, Line 43) with "Portable Operating System Interface (POSIX®, IEEE Std 1003.1^{tm})" for acronym clarification.

r.   Please replace "**time, e.g., a single state from each of a multitude of buses;**" (Paragraph 0033, Line 11) with "time (e.g., a single state from each of a multitude of buses)".

s.   Please define "**WAND**" (Paragraph 0033, Line 16) acronym.

t.   Please define "**WOR**" (Paragraph 0033, Line 16) acronym.

u.   Please replace "**the destination variable(s) <u>248</u>**" (Paragraph 0033, Line

18) with "the destination variable(s) <u>242</u>" to correct error in reference.

v.   Please replace "**itself, e.g., places values on its output "pins"**

accordingly." (Paragraph 0038, Line 8) with "itself (e.g., places values on its

output "pins" accordingly)."

w.   Please replace "**The hardware object, on**" (Paragraph 0038, Line 14)

with "The hardware object 304, on".

x.   Please replace "**CPU object 304**" (Paragraph 0038, Line 24) with

"hardware object 304".

y.   Please replace "**CPU object 304**" (Paragraph 0038, Line 27) with

"hardware object 304".

z.   Please replace "**CPU object 304**" (Paragraph 0038, Line 29) with

"hardware object 304".

Appropriate correction is required.

6.   The use of the trademarks has been noted in this application. They should be

capitalized wherever they appear and be accompanied by the generic terminology when

appropriate.

a.   Please replace "**language, e.g., C, C++, SystemC, and/or Java, or in low level assembly code.**" (Paragraph 0012, Line 5) with "language (e.g., C ®, C++ ®, SystemC ®, and/or Java ®, or in low level assembly code).

b.   Please replace "**written in C**" (Paragraph 0015, Line 9) with "written in C ®".

c.   Please replace "**as a SystemC**" (Paragraph 0016, Line 2) with "as a SystemC ®".

d.   Please replace "**to, SystemC,**" (Paragraph 0016, Line 3) with "to, SystemC ®,".

e.   Please replace "**Verilog, HDL, C, C++, SystemC, Java, or low-level assembly.**" (Paragraph 0018, Line 12) with "Verilog ®, high-level design language (HDL), C ®, C++ ®, SystemC ®, Java ®, or low-level assembly."

f.   Please replace "**SPEEDCompiler**" (Paragraph 0018, Line 14) with "SPEEDCompiler ®".

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks. Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

7.   Claim 23 is objected to because of the following informalities:

    a.   Please replace **"comprising the at least one transactor object"** (Claim

23, Line 1) with "comprising at least one transactor object" to resolve antecedent

issue.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

8.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9.   Claims 1-15 are rejected under 35 U.S.C. 101 because they fail to produce

(claim) a real-world result. Claims 1-26 relate to a method/apparatus of simulating an

object-oriented hierarchal hardware device, however the claimed method/apparatus

does not produce (claim) a real-world result that is useful, tangible, and concrete.

In determining whether the claim is for a "practical application," the focus is not

on whether the steps (components) taken (combined) to achieve a particular result are

useful, tangible, and concrete, but rather that the final result achieved by the claimed

invention is "useful, tangible, and concrete." In the instant application claims 1-26, the

mere simulation of a system does not produce a "useful, tangible, and concrete" result,

and the applicant has not claimed a final result that is "useful, tangible, and concrete"

outside of the simulation method/apparatus its self.

10.   Claims 16-26 are rejected under 35 U.S.C. 101 because they are functional

descriptive material. In this context, "functional descriptive material" consists of data

structures and computer programs, which impart functionality when employed as a

computer component. (The definition of "data structure" is "a physical or logical

relationship among data elements, designed to support specific data manipulation

functions." The New IEEE Standard Dictionary of Electronic Terms 308 (5th ed. 1993).)

        The claims lack the necessary physical articles or objects to constitute a machine

or a manufacture within the meaning of §101. They are clearly not a series of steps or

acts to be a process nor are they a combination of chemical compounds to be a

composition of matter. As such, they fail to fall within a statutory category. They are, at

best, functional descriptive material *per se*.

        Applicant is requested to specifically cite (reference) support in the specification

for claims 1-26 in reference to the method/apparatus claims in response to this office

action without the addition of new subject matter.

Claim Rejections - 35 USC § 112

11.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

12.   Claims 16-26 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter

which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 16-26 consists of an apparatus for conducting the simulation. However, the applicant has failed to disclose in the specification a physical description of the apparatus and its subsequent parts. As a result the applicant has failed to comply with the written description requirement.

Applicant is requested to specifically cite (reference) support in the specification for claims 16-26 in reference to the claims in response to this office action without the addition of new subject matter.

Claim Rejections - 35 USC § 102

13.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14.   Claims 1-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Parson (US 6,053,947 April 25, 2000).

As per claim 1, Parson discloses, "A method for executing a simulation of a hardware device," as ["A method, apparatus, and system for simulating the operation of a circuit (Abstract, Line 1)" and "a method, apparatus, and system of employing an object-oriented programming convention for simulating hierarchical circuits (Column 1, Line 10)] "providing at least one update object" [b) scheduling one or more subcircuit

functions that use the signal for execution according to a priority assigned to each

subcircuit function (Abstract, Line 5)] "having update initialization criteria" [FIG. 3 shows the

relationship of one embodiment having five modeling infrastructure classes: (a) a shell

model 301, (b) an active model 302, (c) a leaf model 303, (d) a clocked model 304 and (e) a

scheduler model 305. Central to the relationships among these models is the concept of

inheritance in an object-oriented language such as C++. For Example, C++ defines

object contents and behaviors in terms of class definitions, where a class definition

states the members objects and member functions (behaviors) found in all objects of

that class. (Column 6, Line 40)] "providing at least one hardware object simulating

functionality associated with at least one hardware device" ["(a) a constructing a simulation

model using an object-oriented programming convention; and (b) simulating the circuit

using the constructed simulation model" (Column 2, Line 37), and "The simulation model

comprises an infra structure of classes that are used to construct objects" (Column 6,

Line 23), and "The classes are divided into basically two groups (1) models and (2)

signals." (Column 6, Line 26), and "The models of the present invention comprise both

generic models and circuit-specific models. The generic models introduce basic

parameters and structure, while circuit-specific models are customized for a particular

circuit." (Column 6, Line 30)] "the at least one hardware object being responsive to the at

least one update object" ["(b) scheduling one or more subcircuit functions that use the

signal for execution according to a priority assigned to each subcircuit function"

(Abstract, Line 5) and "signal values are distributed among interconnected models only

on value changes, and then, only to those non-hierarchical models that use the changed

signal values in their function." (Column 2, Line 43)] "providing at least one master object in

communication with the at least one update object and the at least one hardware object"

["signal values are distributed among interconnected models only on value changes, and then, only to those non-hierarchical models that use the changed signal values in their function." (Column 2, Line 43) and "the process of simulating a circuit comprises distributing a signal only upon a change in the signal, and then only to those simulation models that use the signal" (Column 5, Line 5) and "The clocked model contains a timing function, herein referred to as the "clock0" function, to control the internal state of a leaf model having an internal state. When this function is exercised, the input signal(s) on the leaf model are acknowledged and stored in the leaf model. In this way, the clock0 function controls the leaf model's input(s)" (Column 9, Line 2) and "The scheduler model supports the scheduling feature. It schedules eval0 functions for execution according to their priority. The scheduler model defines eval0 to be a scheduler function that calls a circuit-specific leaf model/clocked model eval0 function in circuit priority-driven sequence" (Column 9, Line 31)] "advancing, by the master object, the at least one update object by a predetermined increment" ["returning to step (a) to repeat the process" (Abstract, Line 11) and "During simulation model functions are scheduled and executed according to their priority" (Column 2, Line 48) and "the data flow feature and scheduling feature cooperate to provide for the efficient propagation and execution of signals in the simulation model" (Column 4, Line 9) and "Each circuit-specific class derived from clocked model should define a clock0 function to update the model's internal state upon a clock input change" (Column 9, Line 25)] "executing the at least one hardware object based at least in part on the incremented update object" ["the data flow feature and scheduling feature cooperate to provide for the efficient propagation and execution of signals in the simulation model" (Column 4, Line 9) and "Each circuit-specific class derived from clocked model should define a clock0 function to update the model's

internal state upon a clock input change" (Column 9, Line 25) and "The scheduler model supports the scheduling feature. It schedules eval0 functions for execution according to their priority. The scheduler model defines eval0 to be a scheduler function that calls circuit-specific leaf model/clocked model eval0 functions in circuit priority-driven sequence." (Column 9, Line 31)]

As per claim 2, Parson discloses, "wherein the update object comprises a clock object" as [The clocked model contains a timing function, herein referred to as the "clock0" function, to control the internal state of a leaf model having an internal state. When this function is exercised, the input signal(s) on the leaf model are acknowledged and stored in the leaf model. In this way, the clock0 function controls the leaf model's input(s). (Column 9, Line 2)

As per claim 3, Parson discloses, "wherein the update object comprises a level object" as [Level transition includes transitions into and out of unknown clock signal values (Column 12, Line 10)].

As per claim 4, Parson discloses, "wherein the update object comprises an arbitrary function object as ["In one embodiment, the active model introduces and defines two specific functions, eval0 and scheduleForEval0." (Column 8, Line 6) and "The scheduler model supports the scheduling feature. It schedules eval0 functions for execution according to their priority." (Column 9, Line 31) and "In addition to holding one or more bits of digital information, the bus signal also contains a function for prompting the leaf models for which it supplies an input to schedule themselves for eval0" (Column 11, Line 4) and "The clock signal's clockThenEvalOnEvent0 function takes two arguments, a pointer to a clocked

model that the signal drives, and a clock transition to which that model is sensitive (Column 12, Line 3).

As per claim 5, Parson discloses, "wherein the update initialization criteria comprise at least one of a clock period, a clock duty cycle, a clock initial value, and a clock offset" as **[Transitions include the values rising, falling, edge and level, which correspond to low-to-high, high-to-low, both low-to-high and high-to-low, or any transition respectively. (Column 12, Line 7).**

As per claim 6, Parson discloses, "wherein the update initialization criteria comprise at least on of a level initial value and a level transition time" as **["C++ defines object contents and behaviors in terms of class definitions, where a class definition states the member objects and member functions (behaviors) found in all objects of the class." (Column 6, Line 46) and "This C++ modeling technology relies on using clock signals driven from outside the bus signal dataflow for generation of digital clocks." (Column 10, Line 38).**

As per claim 7, Parson discloses, "wherein the update initialization criteria comprise a predetermined value corresponding to a predetermined time" as **["C++ defines object contents and behaviors in terms of class definitions, where a class definition states the member objects and member functions (behaviors) found in all objects of the class." (Column 6, Line 46) and "Because such models have the capability of storing one or more input signals, they have an internal state. This type of leaf model stores an input signal(s) at a particular instant and then**

manipulate the signal(s) when its eval0 function is exercised. **This latter leaf model requires a clocked model"** (Column 8, Line 56)].

As per claim 8, Parson discloses, "comprising at least one transactor object associated with the hardware object" as **[Among these properties is inheritance, which refers to the ability of a subclass to inherent properties of the class from which it depends. Another property is aggregation or containment, which refers to the ability to group or contain objects in a hierarchy according to function. And finally, the language should have encapsulation which refers to the ability to incorporate implementation details with objects." (Column 4, Line 18) and "Model constructor interfaces that accept boundary signal addresses as port parameters, and model constructor bodies that build subcircuits by constructing interconnected nested signal and model objects, together provide the notational feature." (Column 12, Line 35)]**

As per claim 9, Parson discloses, "wherein the predetermined increment varies based at least in part on the at least one update object" as **["The bus signal object supports the dataflow feature. More specifically, it connects an output of a leaf model that drives it to one or more leaf models that use it as input, and thus serves as a placeholder for a signal value." (Column 10, Line 60) and "In addition to holding one or more bits of digital information, the bus signal also contains a function for prompting the leaf models for which it supplies an input to schedule themselves" (Column 11, Line 4).**

As per claim 10, Parson discloses, "wherein the predetermined increment varies based at least in part on the at least one update object" as **[The bus signal object supports the dataflow feature. More specifically, it connects an output of a leaf model that drives it to one or more leaf models that use it as input, and thus serves as a placeholder for a signal value. (Column 10, Line 60)].**

As per claim 11, Parson discloses, "wherein the hardware object comprises coding in a high level language" as **["the invention establishes a programming convention for an object-oriented programming language for constructing a simulation model" (Column 3, Line 34) and "Suitable object-oriented language include, for example, C++, Smalltalk, and Java" (Column 4, Line 25)].**

As per claim 12, Parson discloses, "wherein the high-level language comprises at least one of C, C++, SystemC, and Java" as **["the invention establishes a programming convention for an object-oriented programming language for constructing a simulation model" (Column 3, Line 34) and "Suitable object-oriented language include, for example, C++, Smalltalk, and Java" (Column 4, Line 25)].**

As per claim 13, Parson discloses, "wherein the hardware object comprises coding in low-level assembly code" as **[Traditionally, circuits have been described using netlist languages which are well known in the art. (Column 1, Line 29)]**

As per claim 14, Parson discloses, "wherein the transactor comprises an abstract interface and a pin-level interface, the abstract interface being in communication with an execution environment and the pin-level interface being in communication with the hardware object" as **["the language should have encapsulation which refers to the ability to incorporate implementation details within the objects" (Column 4,**

Line22) and "Interfaced with the simulator 205 is a simulation model 206. The

simulation model 206 provides a modular interface, and thus can be "wrapped" to

execute under the control of the simulation 205" (Column 6, Line 4) and "A circuit-

specific shell model class uses its constructor to construct all of the signal and

model objects it contains. It contains those objects that appear as nets and

subcircuits in its hierarchical netlist. The dependent model passes these

parameters to the shell model's constructor. A C++ model object constructor that

conforms to the above notational convention creates a C++ model object

hierarchy that is isomorphic to corresponding hierarchical netlist structure such

as a structural VHDL model." (Column 7, Line 32) and "Model constructor

interfaces that accept boundary signal addresses as port parameters, and model

constructors bodies that build subcircuits by constructing interconnected nested

signal and model objects, together provide the notational feature." (Column 12,

Line 35)]

As per claim 15, Parson discloses, "wherein the hardware object, in

communication with the transactor, comprises a representation of a hardware device"

as ["A circuit-specific shell model class uses its constructor to construct all of

the signal and model objects it contains. It contains those objects that appear as

nets and subcircuits in its hierarchical netlist. The dependent model passes

these parameters to the shell model's constructor. A C++ model object

constructor that conforms to the above notational convention creates a C++

model object hierarchy that is isomorphic to corresponding hierarchical netlist

structure such as a structural VHDL model." (Column 7, Line 32) and "Model

constructor interfaces that accept boundary signal addresses as port parameters,

and model constructors bodies that build subcircuits by constructing

interconnected nested signal and model objects, together provide the notational

feature." (Column 12, Line 35)]

As per claim 16, please see rejection to claim 1.

As per claim 17, please see rejection to claim 2.

As per claim 18, please see rejection to claim 3.

As per claim 19, please see rejection to claim 4.

As per claim 20, please see rejection to claim 5.

As per claim 21, please see rejection to claim 6.

As per claim 22, please see rejection to claim 7.

As per claim 23, please see rejection to claim 8.

As per claim 24, please see rejection to claim 9.

As per claim 25, please see rejection to claim 14.

As per claim 26, please see rejection to claim 15.

Conclusion

15.   In addition to reference used under 35 U.S.C. 102, additional prior art references

that disclose relevant subject matter on the merits can be found in Furuichi (US

5,437,037 July 25, 1995).

Furuichi teaches:

    a.   Simulation program using software language C (Column 1).

    b.   Functions defined in modular form (Column 1).

    c.   Initiation of simulation criteria (Column 2,11).

    d.   Master control object (Column 2,3,4,5).

    e.   Object-oriented programming (Column 3).

    f.   Usage of assembly language (Column 5).

    g.   Usage of an update object (Column 5).

    h.   Time event trigger events (Column 5,6)

    i.   Variable triggered events, variable list (Column 6).

16.   The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

    When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

17.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan R. Plante whose telephone number is (571)

272-9780. The examiner can normally be reached on Monday through Friday 9:00 AM to 4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Pierre M. Vital can be reached on (571) 272-4215. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 17, 2006   Jonathan Plante
JRP   Art Unit 2112

PIERRE VITAL
SUPERVISORY PATENT EXAMINER